Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a load;

a transistor electrically connected to the load; [[and]]

a first switch electrically connected to the transistor;

a second switch electrically connected to the transistor;

a ~~circuit~~ first current source electrically connected to ~~a gate terminal of the transistor,~~ the first switch; and

a second current source electrically connected to the second switch;

wherein ~~the circuit~~ the first current source feeds ~~either~~ a first current [[to]] between the source and the drain of the transistor through the first switch so that the gate terminal of the transistor has a first potential, and

wherein the second current source feeds [[or]] a second current between the source and the drain of the transistor through the second switch so that the gate terminal of the transistor has a second potential~~, and~~

~~wherein the transistor feeds the second current to the load~~.

2. (Currently Amended) A semiconductor device comprising:

a display element;

a transistor electrically connected to the display element; [[and]]

a first switch electrically connected to the transistor;

a second switch electrically connected to the transistor;

a ~~circuit~~ first current source electrically connected to ~~a gate terminal of the transistor,~~ the first switch; and

a second current source electrically connected to the second switch;

wherein the ~~circuit~~ first current source feeds ~~either~~ a first current [[to]] between the source and the drain of the transistor through the first switch so that the gate terminal of the transistor has a first potential, and

wherein the second current source feeds [[or]] a second current [[to]] between the source and the drain of the transistor through the second switch so that the gate terminal of the transistor has a second potential~~, and~~

~~wherein the transistor feeds the second current to the display element~~.

3. (Canceled).

4. (Currently Amended) A semiconductor device comprising:

a load;

a transistor electrically connected to the load; [[and]]

a first switch electrically connected to the transistor;

a second switch electrically connected to the transistor;

a ~~circuit~~ first current source electrically connected to ~~a gate terminal of the transistor,~~ the first switch;

a second current source electrically connected to the second switch;

wherein the ~~circuit~~ first current source feeds ~~either~~ a first current [[to]] between the source and the drain of the transistor through the first switch so that the gate terminal of the transistor has a first potential,

wherein the second current source feeds [[or]] a second current [[to]] between the source and the drain of the transistor through the second switch so that the gate terminal of the transistor has a second potential, and

wherein ~~the transistor feeds~~ a third current flows to the load when the first switch and the second switch are turned off.

5. (Original) The semiconductor device according to claim 4, wherein the load is a display element.

6. (Canceled).

7. (Currently Amended) A semiconductor device comprising:

a load connected in series to a first switch;

a constant current source connected in series to a second switch;

a first power source line electrically connected to the load;

a first transistor electrically connected to the load and the constant current source;

a second transistor electrically connected to the first transistor;

a second power source line electrically connected to the second transistor; and

a third power source line electrically connected to gate electrodes of the first and the second transistors,

wherein the gate electrode of the first transistor is electrically connected to ~~any one of a source electrode of the first transistor and~~ a drain electrode of the first transistor [[via]] through a third switch; and

wherein a source electrode of the second transistor [[are]] is electrically connected to a drain electrode of the second transistor [[via]] through a fourth switch.

8. (Original) The semiconductor device according to claim 7, wherein the load is a display element.

9. (Original) The semiconductor device according to claim 7, wherein the load is a signal line.

10. (Original) The semiconductor device according to claim 7, comprising:

a capacitor electrically connected to the gate electrodes of the first and the second transistors.

11. (Original) The semiconductor device according to claim 7, further comprising a second constant current source electrically connected to the first transistor and connected in series to a fifth switch.

12. (Original) The semiconductor device according to claim 7, wherein a potential of the first power source line is higher than potentials of the second and the third power source lines.

13. (Original) The semiconductor device according to claim 7, wherein a potential of the first power source line is lower than potentials of the second and the third power source lines.

14. (Original) The semiconductor device according to claim 7, wherein widths of channel regions of the first and the second transistors are equal to each other.

15. (Original) The semiconductor device according to claim 7, wherein a length of a channel region of the first transistor is longer than a length of a channel region of the second transistor.

16. (Original) The semiconductor device according to claim 7, wherein the first to fourth switches include any one of a transistor, a diode, a CMOS circuit and a logic circuit.

17. (Withdrawn) A semiconductor device comprising:

a load connected in series to a first switch;

a constant current source connected in series to a second switch;

a first power source line electrically connected to the load;

a first transistor electrically connected to the load and the constant current source;

a second transistor electrically connected to the first transistor;

a second transistor electrically connected to the first transistor;

a second power source line electrically connected to the second transistor; and

a third power source line electrically connected to gate electrodes of the first and the second transistors via a fourth switch,

wherein a gate electrode of the first transistor is electrically connected to any one of a source electrode of the first transistor and a drain electrode of the first transistor via a third switch, and

wherein a gate electrode of the second transistor is electrically connected to the gate electrode of the first transistor via a fifth switch.

18. (Withdrawn) The semiconductor device according to claim 17, wherein the load is a display element.

19. (Withdrawn) The semiconductor device according to claim 17, wherein the load is a signal line.

20. (Withdrawn) The semiconductor device according to claim 17, further comprising a capacitor electrically connected to the gate electrode of the first transistor.

21. (Withdrawn) The semiconductor device according to claim 17, further comprising a second constant current source electrically connected to the first transistor and connected in series to a sixth switch.

22. (Withdrawn) The semiconductor device according to claim 17, wherein a potential of the first power source line is higher than potentials of the second and the third power source lines.

23. (Withdrawn) The semiconductor device according to claim 17, wherein a potential of the first power source line is lower than potentials of the second and the third power source lines.

24. (Withdrawn) The semiconductor device according to claim 17, wherein widths of channel regions of the first and the second transistors are equal to each other.

25. (Withdrawn) The semiconductor device according to claim 17, wherein a length of a channel region of the first transistor is longer than a length of a channel region of the second transistor

26. (Withdrawn) The semiconductor device according to claim 17, wherein the first to fifth switches include any one of a transistor, a diode, a CMOS circuit and a logic circuit.

27. (Withdrawn) A semiconductor device comprising:

a load connected in series to a first switch;

a constant current source connected in series to a second switch;

a first power source line electrically connected to the load;

a first transistor electrically connected to the load and the constant current source and connected to a third switch in series;

a second transistor electrically connected to the load and the constant current source and connected to a fourth switch in series;

a second power source line electrically connected to the first transistor;

a third power source line electrically connected to the second transistor; and

a fourth power source line electrically connected to the load and the constant current source via a fifth switch and electrically connected to gate electrodes of the first and the second transistors.

28. (Withdrawn) The semiconductor device according to claim 27,

wherein the load is a display element.

29. (Withdrawn) The semiconductor device according to claim 27,

wherein the load is a signal line.

30. (Withdrawn) The semiconductor device according to claim 27, comprising

a capacitor electrically connected to gate electrodes of the first and the second transistors.

31. (Withdrawn) The semiconductor device according to claim 27, comprising

a second constant current source electrically connected to the first and the second transistors and connected in series to a sixth switch.

32. (Withdrawn) The semiconductor device according to claim 27,

wherein the potential of the first power source line is higher than potentials of the second, the third, and the fourth power source lines.

33. (Withdrawn) The semiconductor device according to claim 27,

wherein the potential of the first power source lie is lower than potentials of the second, the third, and the fourth power source lines.

34. (Withdrawn) The semiconductor device according to claim 27,

wherein widths of channel regions of the first and the second transistors are equal to each other.

35. (Withdrawn) The semiconductor device according to claim 27,

wherein a length of a channel region of the first transistor is longer than a length of a channel region of the second transistor.

36. (Withdrawn) The semiconductor device according to claim 27,

wherein the first to fifth switches include any one of a transistor, a diode, a CMOS circuit and a logic circuit.

37. (Withdrawn) A semiconductor device comprising:

a load connected in series to a first switch;

a constant current source connected in series to a second switch;

a first power source line electrically connected to the load;

a first transistor electrically connected to the load and the constant current source and connected to a third switch in series;

a second transistor electrically connected to the load and the constant current source and connected to a fourth switch in series;

a second power source line electrically connected to the first transistor;

a third power source line electrically connected to the second transistor; and

a fourth power source line electrically connected to the load and the constant current source via a fifth switch and electrically connected to gate electrodes of the first and the second transistors,

wherein a gate electrode is electrically connected any one of a source electrode of the second transistor and a drain electrode of the second transistor.

38. (Withdrawn) The semiconductor device according to claim 37, wherein the load is a display element.

39. (Withdrawn) The semiconductor device according to claim 37, wherein the load is a signal line.

40. (Withdrawn) The semiconductor device according to claim 37, further comprising a capacitor electrically connected to a gate electrode of the first transistor.

41. (Withdrawn) The semiconductor device according to claim 37, further comprising a second constant current source electrically connected to the first and the second transistors and connected in series to a sixth switch.

42. (Withdrawn) The semiconductor device according to claim 37, wherein a potential of the first power source line is higher than potentials of the second, the third, and the fourth power source lines.

43. (Withdrawn) The semiconductor device according to claim 37,
wherein a potential of the first power source line is lower than potentials of the second, the third, and the fourth power source lines.

44. (Withdrawn) The semiconductor device according to claim 37, wherein widths of channel regions of the first and the second transistors are equal to each other.

45. (Withdrawn) The semiconductor device according to claim 37, wherein a length of a channel region of the first transistor is shorter than a channel region of the second transistor.

46. (Withdrawn) The semiconductor device according to claim 37, wherein the first to fifth switches include any one of a transistor, a diode, a CMOS circuit and a logic circuit.

47. (Currently Amended) A driving method of a semiconductor device, comprising the steps of:

feeding a first current [[to]] between the source and the drain of a transistor through a first switch so that a gate terminal of the transistor has a first potential,

feeding a second current [[to a]] between the source and the drain of the transistor through a second switch so that the gate terminal of the transistor has a second potential, and

feeding ~~the second~~ a third current to a load through the transistor while the gate terminal of the transistor is kept at the second potential when the first switch and the second switch are turned off.

48. (Original) The driving method of a semiconductor device according to claim 47, wherein the first current is larger than the second current.

49. (Currently Amended) A driving method of a semiconductor device comprising the steps of:

feeding a first current [[~~to~~]] between the source and the drain of a transistor through a first switch so that a gate terminal of the transistor has a first potential,

feeding a second current [[~~to a~~]] between the source and the drain of the transistor through a second switch so that the gate terminal of the transistor has a second potential, and

feeding a third current to ~~a load~~ a display element through the transistor while the gate terminal of the transistor is kept at the second potential when the first switch and the second switch are turned off.

50. (Canceled)

51. (Currently Amended) A semiconductor device comprising:

a load;

a transistor electrically connected to the load [[via]] through a first switch;

a first current source;

a second current source; and

a capacitor electrically connected to a gate terminal of the transistor,

wherein any one of a source terminal and a drain terminal of the transistor is connected to the first current source and the second current source [[via]] through a second switch,

wherein the second current source feeds a first current to the transistor so that the gate terminal of the transistor has a first potential, and

wherein the first current source feeds a second current to the transistor so that the gate terminal of the transistor has a second potential[[,]]

~~wherein the transistor feeds the second current to the load~~.

52. (Previously Presented) The semiconductor device according to claim 51, wherein the load is a display element.

53. (Canceled).

54. (New) The driving method of a semiconductor device according to claim 49, wherein the first current is larger than the second current.